



**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO. 63	FILING DATE 10/02/98	GRIGOR	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO. 6100.01117
--------------------	----------------------	--------	----------------------	--------------------------------

TIMOTHY A MARKISON
MARKISON & RECKAMP
SUITE 1015
175 WEST JACKSON BLVD.
CHICAGO IL 60604

LM02/1013

EXAMINER NGUYEN, K

ART UNIT 2774	PAPER NUMBER
------------------	--------------

DATE MAILED: 10/13/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/032,863

Applicant(s)

Grigor

Examiner

Kevin Nguyen

Group Art Unit

2774



☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-41 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-41 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Art Unit: 2774

DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1- 41 rejected under 35 U.S.C. 103(a) as being unpatentable over Kou in view of Zenda (U.S. Patent No. 4,980,678) in view of Zenda (U.S. Patent No. 5,559,525).

3. As to claim 1, 24, and 33, Kou teaches “method and apparatus for driving a plurality of displays simultaneously”. Accordingly, system 10 corresponds to video graphics processing circuit, host computer 12 consists of a processing unit, display memory 36 corresponds to memory and digital storage medium, frame buffer 48 corresponds to memory stores programming instructions of the claims (figure 1, column 4, lines 64-67), which includes:

a) host computer 12 to receive, manipulate, and store the graphics data is ready to be converted into video signals which can be used to drive the display 18a-18n CRT and LCD (figure 1, column 6, lines 20-26). Accordingly, display 18a-18n corresponds to multiple display, host computer 12 corresponds to computing system of claims. The concept taught herein maybe extended to drive any number and any type of display (column 6, lines 29-30) corresponding to the claimed display preferences.

Art Unit: 2774

b) the two displays to be refreshed at two independent and optimal refresh rates (column 8, lines 43-44), a 32 bit data word from butter 38 may be converted into a sequential pixels on the display screen (figure 1, column 6, lines 53-55) corresponds to the revolution of claim. the concepts taught herein may be extended to drive any type of displays (column 6, lines 30), at least partially, on the observation that the shortcomings of the prior art display (column 3, lines 30-31) corresponds to display preferences can be fulfilled in observance of configure properties of the computing system of claim.

c) the exact configuration of interface 30 will depend upon the particular host computer bus 14 used in the system 10 (figure 1-2, column 5, lines 49-51) corresponding to the claimed when the display preference can be fulfilled, configuring the computing system and the at least one of the multiple display in accordance with the display preferences.

4. In regard to claim 2, Zenda (4,980,678) teaches "display controller for CRT/Flat panel display apparatus" which includes keyboard 16 for inputting palette data and various commands (column 3, lines 52-53) and CPU 1 executes rewrite processing of palette 13 in accordance with an application program (figure 1, column 5, lines 36-39) corresponding to the claimed a user interface of the computing system and an application running on the computing system.

5. In regard to claim 3, Kou teaches:

I) this type of panel is termed a Dual Scan panel since the two panel are scanned simultaneously (column 1, lines 65-67) the data displayed on the LCD was directly derived by capturing the sequential data stream targeted for the CRT and converting the data to LDC format

Art Unit: 2774

(column 2, lines 3-6) corresponds to display and image on more than one of the multiple displays.

ii) the display controller 16 simultaneously drives two separate displays (column 6, lines 24-25) corresponding to the claimed displaying separate image on each of the multiple displays.

iii) the dithering pattern was different for the two halves of the screen, thus creating an inferior display (column 9, lines 27-29) corresponding to the claimed display a portion of the image on one of the multiple displays and displaying the image on another one of the multiple displays.

iv) allows the two displays to be refreshed at two independent and optimal refresh rates (column 8, lines 43-44) corresponding to the claimed providing different refresh rates for at least two of the multiple displays.

v) there are two displays with one display being a CRT display and the other display being an LCD (column 5, lines 9-11) corresponding to the claimed providing different resolutions for at least two of the multiple displays.

vi) the display controller 16 simultaneously drives two separate displays (column 6, lines 24-25) video signals (column 6, lines 23) correspond to the claimed selecting a particular one of the multiple displays to display a particular type of image.

Art Unit: 2774

vii) the dithering pattern was different for the two halves of the screen, thus creating an inferior display (column 9, lines 27-29). Accordingly, two halves of the screen corresponds to first portion and second portion of the image of the two display.

6. In regard to claim 4, Zenda (4,980,678) teaches a command is inputs, through keyboard 16, to switch the display apparatus to be used from PDP 21 to CRT 19 (figure 1, figure 6A, column 5, lines 19-21) corresponding to the claimed limitations of the computing system and operational rules of the computing system.

7. In regard to claim 5, 25, and 34 Zenda (4,980,678) teaches step 75, 77, 79, and 81 in figure 11A, step 83, 85, 87, and 89 in figure 11B, CPU 1 rewrites the content of palette 13 to be designated palette data (figure 6A, column 5, lines 15-16) corresponding to the claimed reconfigure display preferences can be fulfilled.

8. In regard to claim 6, Zenda (4,980,678) teaches figures 11A and 11B are flow charts showing display processing performed (column 2, lines 44-45) if display processing did not performed then rewritten loop was error. Accordingly, showing display corresponds to display preferences, did not performed corresponds to cannot be fulfilled, and error corresponds to denial message.

9. In regard to claim 7, 26, and 35, Kou teaches display controller 16 comprise host interface 30 which is the graphics data is ready to be converted into video signals which can be used to drive the display 18a-18n (figure 1 and figure 2, column 6, lines 22-24). Accordingly, display

Art Unit: 2774

controller 16 corresponds to display controller, graphics data corresponds to display data, and display 18a-18n corresponds to multiple displays of claim.

10. In regard to claim 8, 27, and 36, Zenda (4,980,678) teaches CPU 1 reads out display data from VRAM 15 (figure 1, column 5, lines 47-48) in accordance with palette 13 whose content is rewritten with PDP palette data, thereby displaying data on PDP 21 (figure 1, column 5, lines 49-51). Accordingly, VRAM 15 corresponds to screen memory, rewrite corresponds to retrieve, PDP 21 corresponds to one display of the claim.

11. In regard to claim 9, 28, and 37, Zenda (4,980,678) teaches CPU 1 readouts display data from VRAM 15 (column 5, lines 47-48), in step 70, CPU 1 load default value D.CRT of CRT palette data and default value D.PDP of PDP palette data stored in BIOS.ROM 17 into CRT palette data buffer 5 and PDP palette data buffer 7, respectively (figure 1, figure 11A, column 6, lines 61-65) CRT 19 controller (CRTC) 25 selectively display-drives CRT 19 and PDP 21 (column 3, lines 45-46) corresponding to the claimed display drivers writes the separate display data to screen memories.

12. In regard to claim 10, 12, 13, 29, 38, 31, 40, 32, and 41, Zenda (5,559,525) teaches the first display controller 87 is incorporated (figure 3A, column 7, lines 45) and outputs display data P7-0 to be connected RAMDAC 93 and displayed on the color LCD panel 91 (figure 3A column 7, lines 46-67), the second display controller 109 outputs display data to be connected RAMDAC 111 and displayed on the color CRT display unit 107 (figure 3A, column 9, lines 13-15). Accordingly, RAMDAC corresponds to screen memory of the claim.

Art Unit: 2774

13. In regard to claim 11, 30, and 39, Zenda (5,559,525) teaches the first display controller 87 outputs display data 'LP, FP' , 'FR, P7-0', 'PCLK' to be connected RAMDAC 111 and SELECTOR 113 on the color CRT 117 (figure 3A) corresponds to the third display of the claim.

14. In regard to claim 14, Zenda (5,559,525) teaches circuit in figure 3A corresponds to video graphics processing circuit of the claim comprises:

a portable computer capable of selectively displaying image data supplied form two or more display controllers on the flat panel display apparatus (column 1, lines 10-14) corresponds to plurality of display controllers;

a VRAM 11 stores display data to be displayed in color on a color CRT display unit 13 or a color LCD panel 15 (figure 26, column 1, lines 30-33) VRAM corresponds to screen memory of the claims;

analog switch 97 receives the control signals LP, FP, PCLK, and WCLK from the first display controller 87, and outputs them (figure 3A, column 8, lines 20-22). Accordingly, analog switch 97 corresponds to coupling module,

the selector 113 is connected to the first display controller 87 by the feature connector 103, and to the color LCD controllers 95 by the Z connector 105 (figure 3A, column 9, lines 27-29) corresponds to coupling controller of the claimed;

outputs display data P7-0 to be displayed on the color LCD panel 91 and also on the color CRT display unit 89 (figure 3A, column 7, lines 47-49). Accordingly, color panel 91 and CRT display unit 89 corresponds to receive display preferences of the claimed;

Art Unit: 2774

entire configuration of the computer (column 6, lines 45) corresponding to the configuration properties of the claimed;

CPU 1 reads out display data from VRAM 15 (figure 1, column 5, lines 47-48) in accordance with palette 13 whose content is rewritten with PDP palette data, thereby displaying data on PDP 21 (Zenda 4,980,678, figure 1, column 5, lines 49-51). Accordingly, VRAM 15 corresponds to screen memory, rewrite corresponds to retrieve, PDP 21 corresponds to one display of the claim.

15. In regard to claim 15, 16, and 17, Zenda (4,980,678) teaches CPU 1 readouts display data from VRAM 15 (column 5, lines 47-48), in step 70, CPU 1 load default value D.CRT of CRT palette data and default value D.PDP of PDP palette data stored in BIOS.ROM 17 into CRT palette data buffer 5 and PDP palette data buffer 7, respectively (figure 1, figure 11A, column 6, lines 61-65) CRT 19 controller (CRTC) 25 selectively display-drives CRT 19 and PDP 21 (column 3, lines 45-46). Accordingly, VRAM 15 corresponds to plurality of screen memory, D.CRT and D.PDP corresponds to separate display data, display-drives corresponds to display driver, pallet 13 (figure 1) corresponds to graphics engine coupled VRAM and display-drives CRT 19 and PDP 21 of the claimed.

16. In regard to claim 18, Zenda (4,980,678) teaches a command is input through keyboard 16 to switch the display apparatus to be used from PDP 21 to CRT 19 (figure 1, column 5, lines 19-21) by the user (column 5, lines 43). Accordingly, keyboard 16 corresponds to a user interface, PDP 21 and CRT 19 corresponds to display preferences of the claimed.

Art Unit: 2774

17. In regard to claim 19, Zenda (5559525) teaches display data signal can be output by connected first display controller 87 and second display controller 109 through RAMDAC 111' and selector 113' (see figure 3B) corresponding to the claim the plurality of display controllers and the at least on display .

18. In regard to claim 20, Zenda (4,980,678) teaches step 75, 77, 79, and 81 in figure 11A, step 83, 85, 87, and 89 in figure 11B, CPU 1 rewrites the content of palette 13 to be designated palette data (figure 6A, column 5, lines 15-16) corresponding to the claimed reconfigure display preferences can be fulfilled.

19. In regard to claim 21, Zenda (5,559,525) teaches the first display controller 87 is incorporated (figure 3A, column 7, lines 45) and outputs display data P7-0 to be connected RAMDAC 93 and displayed on the color LCD panel 91 (figure 3A column 7, lines 46-67), the second display controller 109 outputs display data to be connected RAMDAC 111 and displayed on the color CRT display unit 107 (figure 3A, column 9, lines 13-15). Accordingly, RAMDAC corresponds to screen memory of the claim.

20. In regard to claim 22, Zenda (5,559,525) teaches the first display controller 87 outputs display data 'LP, FP' , 'FR, P7-0', 'PCLK' to be connected RAMDAC 111 and SELECTOR 113 on the color CRT 117 (figure 3A) corresponds to the third display of the claim.

21. In regard to claim 23, Zenda (U.S. Patent 5,559,525) teaches the first display controller 87 is incorporated (figure 3A, column 7, lines 45) and outputs display data P7-0 to be connected RAMDAC 93 and displayed on the color LCD panel 91 (figure 3A column 7, lines 46-67), the

Art Unit: 2774

second display controller 109 outputs display data to be connected RAMDAC 111 and displayed on the color CRT display unit 107 (figure 3A, column 9, lines 13-15). Accordingly, RAMDAC corresponds to screen memory of the claim.

22. Kou discloses "method and apparatus for driving a plurality of displays simultaneously" which includes display preferences, configuration properties. However, Zenda (4,980,678) discloses CPU 1 rewrites the content of palette 13 to be designated palette data (column 5, lines 15-17). Zenda (5,559,525) discloses first display controller 87 is incorporated (figure 3A, column 7, lines 45) and outputs display data P7-0 to be connected RAMDAC 93 and displayed on the color LCD panel 91 (figure 3A column 7, lines 46-67), the second display controller 109 outputs display data to be connected RAMDAC 111 and displayed on the color CRT display unit 107 (figure 3A, column 9, lines 13-15). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to use the dithering engine must be tightly coupled with the display refresh in order to achieve the maximum benefit of perceived color expansion (Kou, column 2, lines 22-26).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent	4,990,902	Zenda
U.S. Patent	4,990,904	Zenda
U.S. Patent	5,218,274	Zenda

Art Unit: 2774

U.S. Patent	5,293,485	Zenda
U.S. Patent	5,430,457	Zenda
U.S. Patent	5,508,714	Zenda
U.S. Patent	5,592,187	Zenda
U.S. Patent	5,629,715	Zenda

Zenda (5,508,714) is made of record as describing a related "display control apparatus for converting CRT resolution into PDP resolution by hardware".

Zenda (5,218,274) is made of record as describing a related "flat panel display controller using dual-port memory".


22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Nguyen whose telephone number is (703) 305-6209. The examiner can normally be reached on weekdays from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Kevin Nguyen

October 5, 1999



RICHARD A. HJERPE
SUPERVISORY PATENT EXAMINER
GROUP 2700